

Atty. Docket No. Q65962
PATENT APPLICATION

AMENDMENT UNDER 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. - 4. (Cancelled).

5. (New) A voltage subtractor/adder circuit comprising:

a current subtractor and a current-to-voltage converting means providing an output terminal for outputting an output voltage in proportion to the subtraction of two input voltages; and

a differential pair having first and second MOS transistors, both gate electrodes of said first and second MOS transistors forming input terminals for receiving each voltage of said two input voltages, respectively, drain electrodes of said first and second MOS transistors supplying a differential current to said current subtractor, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal for outputting an addition output voltage in proportion to half of the addition of two input voltages;

wherein the sums of currents flowing through said first and second MOS transistors increases in proportion to the square of a difference of said two input voltages; and

a level shifter for level-shifting said addition output voltage from said source electrodes which are commonly coupled.

6. (New) A voltage subtractor/adder circuit comprising:

Atty. Docket No. Q65962
PATENT APPLICATION

AMENDMENT UNDER 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting signals to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal for outputting a voltage to be added;

a constant current source which drives said differential pair; and

a level shifter for level-shifting said addition output voltage from said source electrodes which are commonly coupled.